Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method comprising:

fetching, by a first pipeline of a pipelined processor ~~defining, within a computer program~~, loop conditions corresponding to a particular instance of a loop setup instruction for a first hardware loop;

first propagating a first of said loop conditions of said first hardware loop corresponding to the particular instance of a loop setup instruction via said ~~a~~ first pipeline of a pipelined processor;

piping a second of said loop conditions from said first pipeline of the pipelined processor to a second pipeline of the pipelined processor; and

second propagating in parallel with said first propagating the ~~a~~ second of said loop conditions for said first hardware loop corresponding to the particular instance of a loop setup instruction via said ~~a~~ second pipeline of the pipelined processor.

2. (Previously Presented) The method of claim 1, further comprising:

writing the loop conditions to a first set of registers prior to propagating the loop conditions for said first hardware loop and using said registers to begin calculating parameters based on said loop conditions for said first hardware loop prior to said propagating, and

writing the loop conditions for said first hardware loop to a second different set of registers after propagating the loop conditions, wherein the second different set of registers comprises one or more architectural pipeline registers.

3. (Canceled)

4. (Previously Presented) A method of claim 1, further comprising propagating a third of said loop conditions via a third pipeline.

5. (Original) The method of claim 2, further comprising generating the loop conditions of the hardware loop prior to writing the loop conditions to the first set of registers.

6. (Previously Presented) The method of claim 5, wherein generating the loop conditions comprise calculating at least one of the loop conditions from program counter relative data in the particular instance of the loop setup instruction.

7. (Currently Amended) A method comprising:

first calculating a first loop condition of a first hardware loop from a particular instance of a loop setup instruction using a first arithmetic logic unit in a first pipeline;

second calculating a second loop condition of said first hardware loop from the loop setup instruction using a second arithmetic logic unit in a second pipeline; and

using results of said first calculating and said second calculating for propagating said loop conditions in each of the first and second pipelines ~~loop information~~ to hardware registers associated with calculating parameters of said first hardware loop; and

beginning to calculate said parameters using said first hardware loop, based on said loop conditions, prior to said propagating of said loop conditions in each of the first and second pipelines to the hardware registers.

8. (Original) The method of claim 7, further comprising writing the first and second loop conditions to a first set of registers.

9. (Previously Presented) The method of claim 7, further comprising:

calculating a third loop condition of the hardware loop from the particular instance of the loop setup instruction using a third arithmetic logic unit in a third pipeline; and

writing the first, second and third loop conditions to a first set of registers.

10. (Original) The method of claim 7, wherein calculating the first loop condition and calculating the second loop condition occur in parallel.

11. (Original) The method of claim 8, further comprising propagating the first loop condition to a second set of registers via a first pipeline.

12. (Original) The method of claim 11, further comprising propagating the second loop condition to the second set of registers via a second pipeline.

13. (Currently Amended) An apparatus comprising:

a first pipeline including a first arithmetic logic unit and a second pipeline including a second arithmetic logic unit, and

a control unit coupled to the pipelines, the control unit adapted to:

obtain loop setup instructions for a first hardware loop from a computer program, the loop setup instructions associated with a particular instance of execution of the first hardware loop;

pipe a loop setup instruction from the first pipeline to the second arithmetic unit in the second pipeline;

first calculate a first loop condition of said particular instance of execution of the first hardware loop from one of said loop setup instructions using the first arithmetic logic unit in the first pipeline; and

second calculate a second loop condition of said particular instance of execution of the first hardware loop from the piped a loop setup instruction using the second arithmetic logic unit in the second pipeline, in parallel with said first calculate.

14. (Previously Presented) The apparatus of claim 13, the apparatus further comprising a first set of registers coupled to the control unit, wherein the control unit is further adapted to write the first and second loop conditions of the particular instance of execution of the hardware loop to the first set of registers.

15. (Previously Presented) The apparatus of claim 14, the apparatus further comprising a third pipeline coupled to the control unit, the third pipeline including a third arithmetic logic unit, the control unit further adapted to:

calculate a third loop condition of the particular instance of execution of the hardware loop from the loop setup instruction using the third arithmetic logic unit in the third pipeline; and

write the first, second and third loop conditions of the particular instance of execution of the hardware loop to the first set of registers.

16. (Original) The apparatus of claim 14, the apparatus further comprising a second set of registers coupled to the control unit, wherein the control unit is further adapted to propagate at least one of the loop conditions to the second set of registers via the first pipeline.

17. (Original) The apparatus of claim 16, the control unit further adapted to propagate at least one of the loop conditions to the second set of registers via the second pipeline.

18. (Original) The apparatus of claim 15, the apparatus further comprising a second set of registers coupled to the control unit, the control unit further adapted to:

propagate at least one of the loop conditions to the second set of registers via the first pipeline;

propagate at least one of the loop conditions to the second set of registers via the second pipeline; and

propagate at least one of the loop conditions to the second set of registers via the third pipeline.

19. (Original) The apparatus of claim 14, wherein the first set of registers are speculative registers.

20. (Original) The apparatus of claim 13, wherein at least one of the pipelines is a data address generation pipeline.

21. (Original) The apparatus of claim 13, wherein at least one of the pipelines is a system pipeline.

22. (Currently Amended) An apparatus comprising a set of registers, a first pipeline, and a second pipeline; and

a control unit coupled to the set of registers, the first pipeline and the second pipeline, the control unit adapted to:

first propagate at least one loop condition of a particular instance of execution of a first hardware loop to the set of registers via the first pipeline;

second propagate at least one loop condition of the particular instance of execution of said first hardware loop to the set of registers via the second pipeline; and

begin calculating data using said first hardware loop, prior to propagating the at least one loop condition of a particular instance of execution of said first hardware loop in the first pipeline to the set of registers and prior to propagating the at least one loop condition of the particular instance of execution of said first hardware loop in the second pipeline to the set of registers ~~completing said first and second propagate~~.

23. (Previously Presented) The apparatus of claim 22, wherein the set of registers are a second set of registers, the apparatus further including a first set of registers coupled to the control unit, wherein the control unit is further adapted to:

write the loop conditions of the particular instance of execution of the hardware loop to the first set of registers prior to propagating at least one of the loop conditions to the second set of register.

24. (Original) The apparatus of claim 22, wherein at least one of the pipelines is a data address generation pipeline.

25. (Original) The apparatus of claim 22, wherein at least one of the pipelines is a system pipeline.

26. (Currently Amended) A system comprising:

a static random access memory device;

a processor coupled to the static random access memory device, wherein the processor includes a first set of registers, a first pipeline, a second pipeline, and a control unit adapted to:

pipe a loop setup instruction from the first pipeline to a second arithmetic unit in the second pipeline;

first calculate a first loop condition of a particular instance of execution of a first hardware loop from the ~~a~~ loop setup instruction using a first arithmetic logic unit in the first pipeline;~~,~~

second calculate a second loop condition of said particular instance of execution of the first hardware loop from the loop setup instruction using the ~~a~~ second arithmetic logic unit in the second pipeline, in parallel with the first calculate; and

write the first and second loop conditions of said particular instance of execution of the first hardware loop to the first set of registers.

27. (Previously Presented) The system of claim 26, the processor including a third pipeline, the control unit further adapted to:

calculate a third loop condition of the particular instance of execution of the hardware loop from the loop setup instruction using a third arithmetic logic unit in the third pipeline; and

write the first, second and third loop conditions of the particular instance of execution of the hardware loop to the first set of registers.

28. (Currently Amended) A system comprising:

a static random access memory device;

a processor coupled to the static random access memory device, wherein the processor includes a first set of registers, a second set of registers, a first pipeline, a second pipeline, and a control unit adapted to:

write loop conditions of a first hardware loop to the first set of registers;

propagate at least one of the loop conditions of said first hardware loop to the second set of registers via the first pipeline;

propagate at least one of the loop conditions of said first hardware loop to the second set of registers via the second pipeline; and

begin calculating data using said first hardware loop prior to propagation of the at least one of the loop conditions of said first hardware loop in the first pipeline to the second set of registers and prior to propagation of the at least one of the loop conditions of said first hardware loop in the second pipeline to the second set of registers ~~completing said first and second propagate~~.

29. (Original) The system of claim 28, the processor further including a third pipeline, the control unit further adapted to propagate at least one of the loop conditions to the second set of registers via the third pipeline.

30. (Original) The system of claim 28, the control unit further adapted to:

calculate a first loop condition of the hardware loop from a loop setup instruction using a first arithmetic logic unit in the first pipeline; and

calculate a second loop condition of the hardware loop from the loop setup instruction using a second arithmetic logic unit in the second pipeline.